Processes and Structures for Self-Aligned Contact Non-Volatile Memory with Peripheral Transistors Easily Modifiable for Various Technologies and Applications

ABSTRACT OF THE DISCLOSURE

[37] Structures and methods for flash memory transistors are formed with self-aligned drain/source contacts. The flash transistors are formed with a plurality of gate layers. An etch resistant layer(s) are deposited on top of the gate layers in the memory array transistors and on the gate layers of peripheral transistors. An additional oxide layer/spacer may be formed on the etch resistant layer to control the resulting transistor junction configuration. As a result within the same process various transistors may be formed satisfying various requirements. Contact holes to the drain and source regions of the memory and peripheral transistors are then formed. The etch resistant layer prevents the contact etchants from completely etching away the protective etch resistant layer surrounding the gate layers. The spacing between the drain/source contacts and the gate layers can be greatly reduced increasing the density of the memory array transistors and reducing chip size.